dividing the input clock, a control circuit (102 of Fig.3) for generating a control signal for adding or subtracting to or from a phase by a unit phase differential relative to the input clock with respect to the frequency-divided clocks based on the frequency divided clocks' output from the frequency divider, and a phase adjustment circuit (101 of Fig.3) fed with the input clock and generating and outputting an output clock having a phase prescribed by the control signal from the control circuit.--

A3

IN THE CLAIMS:

Please amend claims 1, 28 and 33-35 to read as follows:

A4

1. (Amended) A clock control circuit comprising:

a circuit for generating and outputting an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of a phase differential on each clock cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock.

A5

28. (Amended) A clock control method comprising the steps of:

generating an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a unit value of a phase differential on each clock cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock; and

outputting said output clock.

A6

33. (Amended) A clock control method comprising the steps of:

generating an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a unit value of a phase differential on each clock cycle of

HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

said reference clock, said reference clock being an input clock or a clock derived from the input clock; and

outputting said output clock wherein the output clock is phase-adjusted by an interpolator outputting a signal, a propagation delay of said signal corresponding to division of timing difference of two clock signals to vary ration of internal division of timing difference of said interpolator to enable outputting of an output clock of a frequency which is a non-integer frequency of the input clock frequency.

34. (Amended) A clock control circuit comprising:

A6

a circuit that receives an input clock and generates an output clock with a phase relative to a reference clock being changed on each cycle of the output clock, said reference clock being the input clock or a clock derived from the input clock, wherein a phase of the output clock relative to the reference clock for another cycle next to one cycle is produced by adding to the phase of the output clock corresponding to said one cycle a unit phase differential value $\Delta\Phi$, where the $\Delta\Phi$ is a predetermined value such that $n\Delta\Phi$ is equal to one clock period(tCK) of said reference clock while said n is a positive integer, and whereby a frequency of the output clock is $1/(tCK+\Delta\Phi)$.

35. (Amended) A clock control circuit comprising:

a circuit that receives an input clock and generates an output clock with a phase relative to a reference clock being changed on each cycle of the output clock, said reference clock being the input clock or a clock derived from the input clock, wherein a phase of the output clock relative to the reference clock for another cycle next to one cycle is produced by subtracting from the phase of the output clock corresponding to said one cycle a unit phase differential value $\Delta\Phi$, where the $\Delta\Phi$ is a predetermined value such that $n\Delta\Phi$ is equal to one clock period (tCK) of said

HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643